WHAT IS CLAIMED IS:

1. A MOS transistor with reduced drain capacitance comprising

a drain, and

a lateral isolation trench extending at least partially underneath the drain.

2. A MOS transistor of claim 1, wherein the trench is filled with air.

3. A MOS of claim 1, wherein the trench is filled with an insulator.

4. A MOS of claim 3, wherein the insulator is a high step coverable insulating material.

5. A MOS of claim 4, wherein the insulator is PETEOS.

6. A MOS of claim 1, wherein the trench has a <110> orientation.

7. A MOS of claim 6, wherein the trench is formed in a <100> silicon wafer.

8. A method of forming a laterally extending trench in a semiconductor material underneath a drain of a MOS transistor, comprising

choosing a predetermined crystal orientation,

etching a vertically extending STI region next to the drain, and

using an anisotropic etchant to etch a trench extending laterally from the STI.

9. A method of claim 8, wherein choosing the crystal orientation includes choosing a wafer with a <100> orientation.

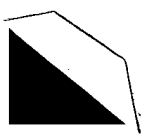
10. A method of claim 8, wherein the choosing of the crystal orientation includes choosing a lateral trench direction that is in the <110> direction.

11. A method of claim 10, wherein the semiconductor material is silicon.

12. A method of claim 11, wherein the etchant is a wet anisotropic silicon etchant.

13. A method of claim 12, wherein the etchant includes KOH.

14. A method of claim 13, wherein the etchant further includes alcohol and water.



15. A method of claim 12, wherein the etchant includes TMAH.